Datasheet

IMPINJ®

MONZA® R6-P

TAG CHIP DATASHEET

IPJ-W1710-K00

Version 2.0

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OVERVIEW

The Monza® R6-P RAIN RFID tag chip is optimized for serializing items such as apparel, electronics, cosmetics, pharmaceuticals, jewelry and various other products. It delivers unmatched read performance and data integrity for effective Item Intelligence applications and record-breaking encoding performance to enable the lowest applied tag cost. With the addition of user memory and range-reduction switch, advanced usages such as loss prevention, brand protection and enhanced privacy are enabled. The Monza R6-P tag chip includes revolutionary technologies such as automatic performance adjustments and encoding diagnostics that reinforce the position of the Monza tag chip family as the RFID industry leader

FEATURES

- Industry leading read sensitivity of up to -22.1 dBm with a dipole antenna, combined with excellent interference rejection, delivers exceptional read reliability
- Superior write sensitivity of up to –17.3 dBm with a dipole antenna for unparalleled encoding reliability
- Inlay compatibility between all Monza 6 family of tag chips (Monza R6, Monza R6-P and Monza S6-C)
- Fast memory write speed of 1.6 ms for 32 bits
- Encoding throughput up to 9,500 tags/minute using the Impinj ItemEncode™ software
- Up to 128-bits of EPC memory
- 96 bits of Serialized TID with 48-bit serial number
- Up to 64 bits of user memory
- RAIN RFID / ISO 18000-63 and EPCglobal Gen2v2 compliant
- Unmatched data integrity with Integra™ Technology for encoding diagnostics
- Maintains performance across different dielectrics with AutoTune™ Technology
- Reduced tag manufacturing variability via Enduro™ Technology
- FastID™ mode enables 2x to 3x faster EPC+TID inventory for authentication and other TID-based applications
- TagFocus™ mode suppresses previously read tags to enable capture of more tags
- Scalable serialization built-in with Monza Self-Serialization
- Impinj's field-rewritable NVM, optimized for RFID, provides 100,000-cycle or 50-year retention reliability
- Enhanced privacy, loss prevention, brand protection

TABLE OF CONTENTS

1 INTRODUCTION

1.1 Scope

This datasheet defines the physical and logical specifications for Gen 2-compliant Monza R6-P tag silicon, a reader-talks-first, radio frequency identification (RFID) component operating in the UHF frequency range.

1.2 Reference Documents

EPC™ Radio Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz (Gen 2 Specification). The conventions used in the Gen 2 Specification (normative references, terms and definitions, symbols, abbreviated terms, and notation) were adopted in the drafting of this Monza R6-P Tag Chip Datasheet. Users of this datasheet should familiarize themselves with the Gen 2 Specification.

Impinj Monza R6-P Wafer Specification

Impinj Monza Wafer Map Orientation

EPC™ Tag Data Standards Specification 1.7

EPCglobal "Interoperability Test System for EPC Compliant Class-1 Generation-2 UHF RFID Devices" v.1.2.4, August 4, 2006. (Monza R6-P tag chips are compliant with this Gen 2 interoperability standard.)

2 FUNCTIONAL DESCRIPTION

The Monza R6-P tag chip fully supports all requirements of the Gen 2 specification as well as many optional commands and features (see Section 2.3 below). In addition, the Monza tag chip family provides a number of enhancements:

- Superior sensitivity for high read and write reliability
- Industry-leading memory write speed, delivering the highest encoding rates
- TagFocus™ inventory mode, a Gen 2 compliant method for capturing more hard-to-read tags by suppressing those that have already been read, by extending their S1 flag B-state
- FastID™ inventory mode, a Gen 2 compliant, patent-pending method for EPC+TID based inventory that is 2-3 times faster than previous methods
- A patent-pending Enduro™ technology makes inlay manufacture less sensitive to die-attach pressure, resulting in less variance and more predictable performance in final inlay product
- AutoTune™ technology allows Monza R6-P inlays to maintain high performance independent of the tagged items dielectric. In addition smaller form factor designs can meet bandwidth requirements with AutoTune. Smaller antennas reduce manufacturing cost and increase the number of applications.
- Integra™ technology, a suite of diagnostics which ensures consistently accurate data delivery that business can depend on

2.1 Memory

Optimized for item-level tagging, the Monza R6-P tag chip offers EPC memory of up to 128 bits, serialized TID, and up to 64 bits of user memory. See Table 2-1 for the memory organization.

Table 2-1 Monza R6-P Memory Organization

MEMORY SECTION	DEFAULT MEMORY PROFILE	MAX USER MEMORY PROFILE
User	32 bits	64 bits
TID (not changeable)	Serial Number—48 bits	Serial Number—48 bits
	Extended TID Header—16 bits	Extended TID Header—16 bits
	Company/Model Number—32 bits	Company/Model Number—32 bits
EPC	128 bits	96 bits
Reserved	Chip Configuration	Chip Configuration
	Kill Password – 32 bits	Kill Password – 32 bits
	Access Password – 32 bits	Access Password – 32 bits

2.2 Advanced Monza Features Support More Effective Inventory

Monza tag chips support two unique, patent-pending features designed to boost inventory performance for traditional EPC and TID-based applications:

- TagFocus™ mode minimizes redundant reads of strong tags, allowing the reader to focus on weak tags that are typically the last to be found. Using TagFocus™, readers can suppress previously read tags by indefinitely refreshing their S1 B state.
- FastID™ mode makes TID-based applications such as authentication practical by boosting TID-based inventory speeds by 2 to 3 times. Readers can inventory both the EPC and the TID without having to perform an access command. Setting the EPC word length to zero enables TID-only serialization.

2.3 Support for Optional Gen 2 Commands

Monza R6-P tag chips support the optional commands listed in Table 2-2.

Table 2-2 Supported Optional Gen 2 Specification Commands

COMMAND	CODE	LENGTH (BITS)	DETAILS
BlockWrite	11000111	>57	• Accepts valid one-word commands • Accepts valid two-word commands if pointer is an even value • Returns error code (00000000_2) if it receives a valid two-word command with an odd value pointer • Returns error code (00000000_2) if it receives a command for more than two words • Does not respond to block write commands of zero words
BlockPermalock	11000111	>66	• User memory when configured to 64 bits • Two blocks, each 32 bits • Ignored when user memory configured to 32 bits
Lock	11000101	60	• Monza R6-P supports the full functionality of the lock Command • Separately lockable EPC and User memory bank • Separately lockable Access and Kill passwords • The TID memory bank is perma-locked read only

2.4 Data Integrity Features (Integra™ technology)

Monza R6-P has several data integrity features that enhance encoding and data reliability. These features include memory self-check, TID parity, and the MarginRead command.

2.4.1 Memory Self-Check

Monza R6-P performs a memory check on its NVM at every power-up. If a bit is weakly encoded an internal flag is set. When the tag is singulated it will respond back with a zero length EPC. A reader could then consider this tag for exception handling.

2.4.2 TID Parity

Monza R6-P is encoded with even parity over the 48 bit serial number portion of the TID. A reader should calculate even parity with bitwise exclusive-OR as follows.

- X = TID bit(30_h) ⊕ TID bit(31_h) ⊕ … ⊕ TID bit($5E_h$) ⊕ TID bit($5F_h$)
- If X = 0 the TID data is good
- If X = 1 the TID data has an error in it

2.4.3 MarginRead Command

The tables below provide details about the custom Impinj MarginRead command.

Table 2-3 MarginRead Command Code

COMMAND	CODE	LENGTH (BITS)	DETAILS
MarginRead	1110000000000001	≥67	• The MarginRead command allows checking for sufficient write margin of known data • The tag must be in the OPEN/SECURED state to respond to the command • If a tag receives a MarginRead command with an invalid handle, it ignores that command • The tag responds with the Insufficient Power error code if the power is too low to execute a MarginRead • The tag responds with the Other error code if the margin is bad for a bit in the mask or if a non-matching bit is sent by the reader • The MarginRead command is only applicable for programmable sections of the memory

Table 2-4 MarginRead Command Details

MARGINREAD COMMAND	CODE	MEM BANK	BIT POINTER	LENGTH	MASK	RN	CRC-16
#bits	16	2	EBV	8	Variable	16	16
Details	11100000 00000001	00: Reserved 01: EPC 10: TID 11: User	Starting Bit Address Pointer	Length in Bits	Mask Value	handle	

Table 2-5 MarginRead Command Field Descriptions

FIELD	DESCRIPTION
Mem Bank	• The memory bank to access.
Bit Pointer	• An EBV that indicates the starting bit address of the mask
Length	• Length of the mask field from 1-255. • A value of zero shall result in the command being ignored
Mask	• This field must match the expected values of the bits • The chip checks that each bit matches what is in the mask field with margin
RN	• The tag will ignore any MarginRead command received with an invalid handle

The tag response to the MarginRead Command uses the preamble specified by the TRext value in the Query command that initiated the round. See Table 2-6 for tag response details.

Table 2-6 Tag Response to a passing MarginRead Command

	HEADER	RN	CRC-16
#bits	1	16	16
Description	0	handle	

2.4.4 Recommended MarginRead Usage Guidelines

There are several ways that the MarginRead command could be used with Monza R6-P. Monza R6-P comes pre-serialized and the MarginRead command allows a programming reader to check that the pre-serialized data is well written and does not need to be re-encoded. Another recommended use of MarginRead is secondary and independent verification of the encoding quality. MarginRead can also be used for diagnosis when doing failure

analysis on tags. The MarginRead command obeys all locking and will return an error code on read locked passwords.

2.5 Monza R6-P Tag Chip Block Diagram

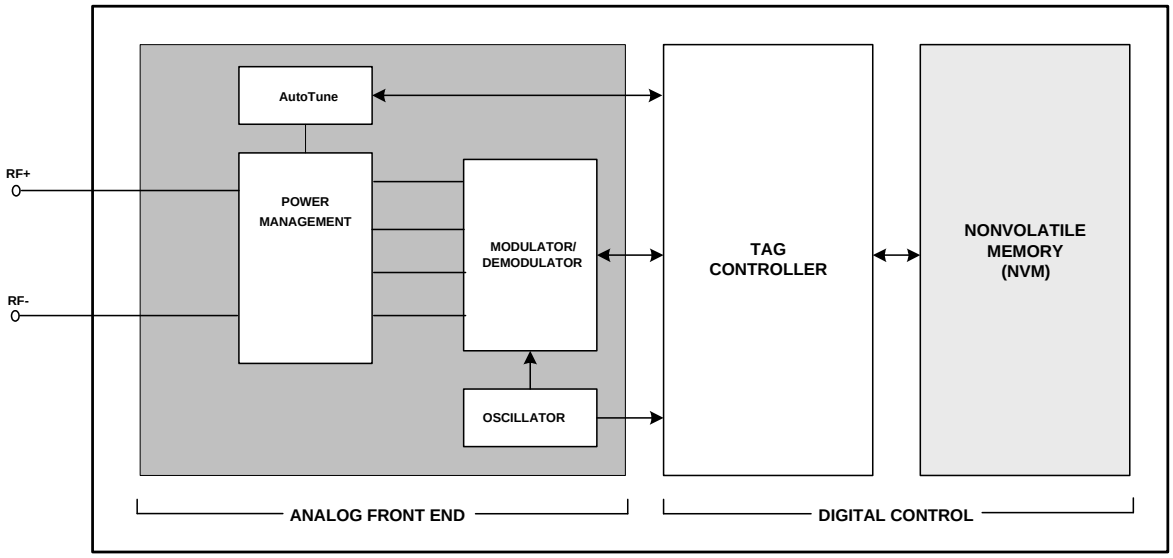

Figure 2-1 Block Diagram

2.6 Pad Descriptions

Monza R6-P tag chips have two external pads available to the user: one RF+ pad, and one RF- pads. RF+ and RF- form a single differential antenna port, as shown in Table 2-7 (see also Figure 2-1 and Figure 2-2). Note that none of these pads connects to the chip substrate.

Table 2-7 Pad Descriptions

EXTERNAL SIGNALS	EXTERNAL PAD	DESCRIPTION
RF+	1	Differential RF Input Pads for Antenna.
RF-	2	

2.7 Differential Antenna Input

All interaction with the Monza R6-P tag chip, including generation of its internal power, air interface, negotiation sequences, and command execution, occurs via its differential antenna port. The differential antenna port is connected with the RF+ pad connected to one terminal and the RF- pad connected to the other terminal.

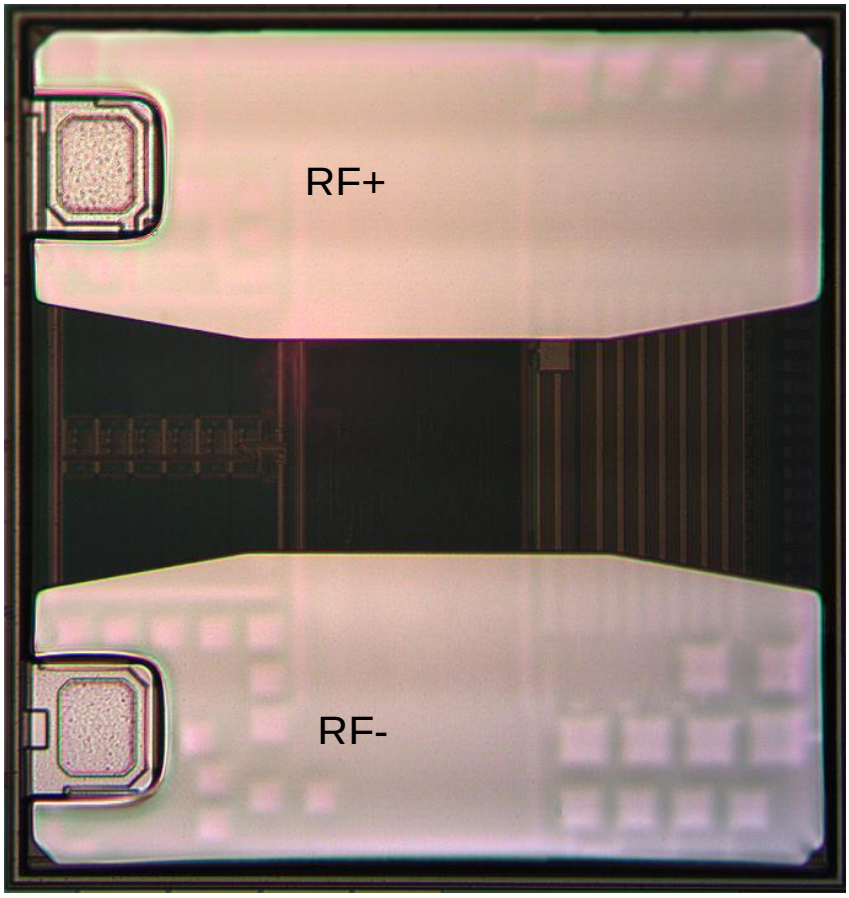

Figure 2-2 Monza R6-P tag chip die orientation

2.8 Monza 6 Antenna Reference Designs

All Monza 6 family of tag chips (Monza R6, Monza R6-P, and Monza S6-C) are designed to be drop-in compatible for antenna inlay designs. Impinj has a set of reference designs available for use by Monza customers under terms of the Impinj Antenna License Agreement.

These reference designs are available here:

https://support.impinj.com/hc/en-us/sections/200454558-Monza-Reference-Design-Documents-Downloads

These documents are restricted. To gain access if these documents cannot be accessed, submit a request for access using the following link. Make sure to select the option “Monza Antenna Reference Designs”.

https://access.impinj.com/prtlaccessrequest

2.9 Monza R6-P Tag Chip Dimensions

Chip dimensions

- 464.1 µm x 442 µm rectangular die size
- 166 µm x 422 µm pad size
- 112 µm pad spacing at center of die
- 154 µm pad spacing at edge of die

2.10 Power Management

The tag is activated by proximity to an active reader. When the tag enters a reader's RF field, the Power Management block converts the induced electromagnetic field to the DC voltage that powers the chip.

2.11 AutoTune

The AutoTune block adjusts Monza R6-P power harvesting from the inlay antenna by adjusting the chip's input capacitance. This adjustment occurs at power up and is held for the remainder of the time that Monza R6-P is powered.

2.12 Modulator/Demodulator

The Monza R6-P tag chip demodulates any of a reader's three possible modulation formats, DSB-ASK, SSB-ASK, or PR-ASK with PIE encoding. The tag communicates to a reader via backscatter of the incident RF waveform by switching the reflection coefficient of its antenna pair between reflective and absorptive states. Backscattered data is encoded as either FM0 or Miller subcarrier modulation (with the reader commanding both the encoding choice and the data rate).

2.13 Tag Controller

The Tag Controller block is a finite state machine (digital logic) that carries out command sequences and also performs a number of overhead duties.

2.14 Nonvolatile Memory

The Monza R6-P tag chip embedded memory is nonvolatile memory (NVM) cell technology, specifically optimized for exceptionally high performance in RFID applications. All programming overhead circuitry is integrated on chip. Monza R6-P tag chip NVM provides 100,000 cycle endurance or 50-year data retention.

The NVM block is organized into three segments:

- EPC Memory with up to 128 bits
- User Memory with up to 64 bits
- Reserved Memory.

The ROM-based Tag Identification (TID) memory contains the EPCglobal class ID, the manufacturer identification, and the model number. It also contains an extended TID consisting of a 16-bit header and 48-bit serialization.

3 INTERFACE CHARACTERISTICS

This section describes the RF interface of the tag chip and the modulation characteristics of both communication links: reader-to-tag (Forward Link) and tag-to-reader (Reverse Link).

3.1 Making Connections

Figure 3-3 shows antenna connection for Monza R6-P tag chips.

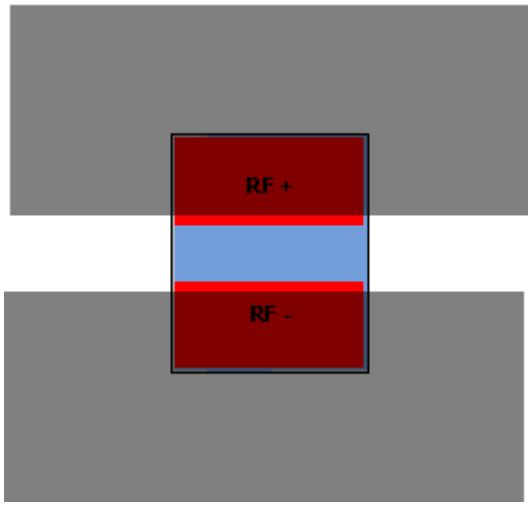

Figure 3-3: Antenna Connection for Inlay Production

This connection configuration for inlay production contacts the Monza R6-P tag chip RF+ pad to one antenna terminal and the RF- pad to the opposite polarity terminal. Enduro pads allow relatively coarse antenna geometry, and thus enable relaxed resolution requirements for antenna patterning compared to bumped products. The diagram in Figure 3-3 shows the recommended antenna trace arrangement and chip placement – having antenna traces partially overlapping the Enduro pads but not extending into the clear space between Enduro pads.

3.2 Impedance Parameters

In order to realize the full performance potential of the Monza R6-P tag chip, it is imperative that the antenna present the appropriate impedance at its terminals. A simplified lumped element tag chip model, shown in Figure 3-4, is the conjugate of the optimum source impedance, which is *not* equal to the chip input impedance. This indirect, source-pull method of deriving the port model is necessary due to the non-linear, time-varying nature of the tag RF circuits. The model is a good mathematical fit for the chip over a broad frequency range. The lumped element values are listed in Table 3-8, where C_{mount} is the parasitic capacitance due to the antenna trace overlap with the chip surface, C_p appears at the chip terminals and is intrinsic to the chip, and R_p represents the energy conversion and energy absorption of the RF circuits.

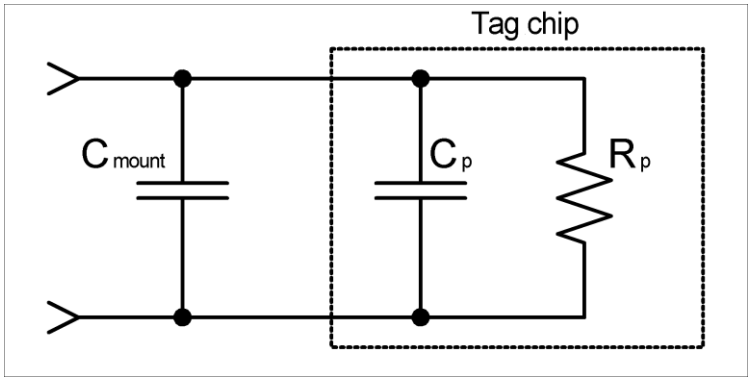

Figure 3-4: Tag Chip Linearized RF Model

Table 3-8 shows the values for the chip port model for the Monza R6-P tag chip, which apply to all frequencies of the primary regions of operation (North America, Europe, and Japan).

Table 3-8 Chip Port Parameters

PARAMETER	TYPICAL VALUE	COMMENTS
C_p	1.23 pF	Intrinsic chip capacitance when AutoTune is mid-range, including Enduro pads.
R_p	1.2 kOhm	Calculated for linearized RF model shown in Figure 3-2. Measured R_p = 1.56 kOhm using network analyzer.
C_{mount}	0.21 pF	Typical capacitance due to adhesive and antenna mount parasitics. Total load capacitance presented to antenna model of Figure 3-2 is: $C_p + C_{mount}$
Chip Read Sensitivity	- 20 dBm	Measured at 25 °C; R=>T link using DSB-ASK modulation with 90% modulation depth, Tari=25 µs, and a T=>R link operating at 170 kbps with Miller M=8 encoding.
Chip Write Sensitivity	- 15.2 dBm	

3.3 Reader-to-Tag (Forward Link) Signal Characteristics

Table 3-9 Forward Link Signal Parameters

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	COMMENTS
RF Characteristics					
Carrier Frequency	860		960	MHz	North America: 902–928 MHz Europe: 865–868 MHz
Maximum RF Field Strength			+20	dBm	Received by a tag with dipole antenna while sitting on a maximum power reader antenna
Modulation		DSB-ASK, SSB-ASK, or PR-ASK			Double and single sideband amplitude shift keying; phase-reversal amplitude shift keying
Data Encoding		PIE			Pulse-interval encoding
Modulation Depth	80		100	%	(A-B)/A, A=envelope max., B=envelope min.
Ripple, Peak-to-Peak			5	%	Portion of A-B
Rise Time ($t_{r,10\text{-}90\%}$)	0		0.33Tari	sec	
Fall Time ($t_{f,10\text{-}90\%}$)	0		0.33Tari	sec	
Tari[1]	6.25		25	µs	Data 0 symbol period
PIE Symbol Ratio	1.5:1		2:1		Data 1 symbol duration relative to Data 0
Duty Cycle	48		82.3	%	Ratio of data symbol high time to total symbol time
Pulse Width	MAX(0.265Tari,2)		0.525Tari	µs	Pulse width defined as the low modulation time (50% amplitude)

3.4 Tag-to-Reader (Reverse Link) Signal Characteristics

Table 3-10 Reverse Link Signal Parameters

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	COMMENTS
Modulation Characteristics					
Modulation		ASK			FET Modulator
Data Encoding		Baseband FM0 or Miller Subcarrier			
Change in Modulator Reflection Coefficient $\|\Delta\Gamma\|$ due to Modulation		0.8			$\|\Delta\Gamma\| = \|\Gamma_{reflect} - \Gamma_{absorb}\|$ (per read/write sensitivity, Table 3-8)
Duty Cycle	45	50	55	%	
Symbol Period[1]	1.5625		25	µs	Baseband FM0
	3.125		200	µs	Miller-modulated subcarrier
Miller Subcarrier Frequency[1]	40		640	kHz	

Note 1: Values are nominal minimum and nominal maximum, and do not include frequency tolerance. Apply appropriate frequency tolerance to derive absolute periods and frequencies.

4 TAG MEMORY

4.1 Monza R6-P Tag Chip Memory Map

Table 4-11 Physical/Logical Memory Map – Default Memory Profile

MEMORY BANK NUMBER	MEMORY BANK NAME	MEMORY BANK BIT ADDRESS	BIT NUMBER															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11_2	User (NVM)	10_h-$1F_h$	User[15:0]															
		00_h-$0F_h$	User[31:16]															
10_2	TID (ROM)	50_h-$5F_h$	TID_Serial[15:0]															
		40_h-$4F_h$	TID_Serial[31:16]															
		30_h-$3F_h$	TID_Serial[47:32]															
		20_h-$2F_h$	Extended TID Header															
		10_h-$1F_h$	Manufacturer ID						Model Number									
		00_h-$0F_h$	1	1	1	0	0	0	1	0	Manufacturer ID							
01_2	EPC (NVM)	90_h-$9F_h$	EPC[15:0]															
		80_h-$8F_h$	EPC[31:16]															
		70_h-$7F_h$	EPC[47:32]															
		60_h-$6F_h$	EPC[63:48]															
		50_h-$5F_h$	EPC[79:64]															
		40_h-$4F_h$	EPC[95:80]															
		30_h-$3F_h$	EPC[95:80]															
		20_h-$2F_h$	EPC[127:111]															
		10_h-$1F_h$	Protocol-Control Bits (PC)															
		00_h-$0F_h$	CRC-16															
00_2	RESERVED (NVM)	140_h-$14F_h$	RFU[12:0]=000_h													ATV[2:0]		
		60_h-$6F_h$	Factory Calibration B [14:0]															
		50_h-$5F_h$	Factory Calibration A [14:0]															
		40_h-$4F_h$	Internal Configuration [15:3]													M	S	A
		30_h-$3F_h$	Access Password[15:0]															
		20_h-$2F_h$	Access Password[31:16]															
		10_h-$1F_h$	Kill Password[15:0]															
		00_h-$0F_h$	Kill Password[31:16]															

Table 4-12 Physical/Logical Memory Map – Max_User Memory Profile

MEMORY BANK NUMBER	MEMORY BANK NAME	MEMORY BANK BIT ADDRESS	BIT NUMBER															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11_2	User (NVM)	30_h-$3F_h$	User[15:0]															
		20_h-$2F_h$	User[31:16]															
		10_h-$1F_h$	User[47:32]															
		00_h-$0F_h$	User[63:48]															
10_2	TID (ROM)	50_h-$5F_h$	TID_Serial[15:0]															
		40_h-$4F_h$	TID_Serial[31:16]															
		30_h-$3F_h$	TID_Serial[47:32]															
		20_h-$2F_h$	Extended TID Header															
		10_h-$1F_h$	Manufacturer ID						Model Number									
		00_h-$0F_h$	1	1	1	0	0	0	1	0	Manufacturer ID							
01_2	EPC (NVM)	70_h-$7F_h$	EPC[47:32]															
		60_h-$6F_h$	EPC[63:48]															
		50_h-$5F_h$	EPC[79:64]															
		40_h-$4F_h$	EPC[95:80]															
		30_h-$3F_h$	EPC[95:80]															
		20_h-$2F_h$	EPC[127:111]															
		10_h-$1F_h$	Protocol-Control Bits (PC)															
		00_h-$0F_h$	CRC-16															
00_2	RESERVED (NVM)	140_h-$14F_h$	RFU[12:0]=000_h													ATV[2:0]		
		60_h-$6F_h$	Factory Calibration B [14:0]															
		50_h-$5F_h$	Factory Calibration A [14:0]															
		40_h-$4F_h$	Internal Configuration [15:3]													M	S	A
		30_h-$3F_h$	Access Password[15:0]															
		20_h-$2F_h$	Access Password[31:16]															
		10_h-$1F_h$	Kill Password[15:0]															
		00_h-$0F_h$	Kill Password[31:16]															

4.2 Logical vs. Physical Bit Identification

For the purposes of distinguishing most significant from least significant bits, a logical representation is used in this datasheet where MSBs correspond to large bit numbers and LSBs to small bit numbers. For example, Bit 15 is the logical MSB of a memory row in the memory map. Bit 0 is the LSB. A multi-bit word represented by WORD[N:0] is interpreted as MSB first when read from left to right. This convention should not be confused with the physical bit address indicated by the rows and column addresses in the memory map; the physical bit address describes the addressing used to access the memory.

4.3 Memory Banks

Described in the following sections are the contents of the NVM and ROM memory, and the parameters for their associated bit settings.

4.3.1 Reserved Memory

Reserved Memory contains the Access and Kill passwords, which are programmed to zero. It also contains three user configuration bits, which may only be changed in the secured state.

- M = the memory map selection bit. This bit is set to one at the factory and may be written once to change the memory map.
- S = the short range bit. This bit is set to zero at the factory. When set this bit puts the chip into a short range mode. The chip will not respond at all unless it is in short range.
- A = the AutoTune disable bit. When the AutoTune disable bit is zero AutoTune works as normal. When the bit is one, AutoTune is disabled and the capacitance on the front end assumes the mid-range value.

To write any one of these three bits a Write command or single word BlockWrite command must be issued to word 4 of reserved memory. The bits of the payload that correspond to the Internal Configuration will be ignored by the tag. The AutoTune value is marked ATV[2:0] in word 14_h. The AutoTune value represents the tuning capacitance scale, from zero to four.

4.3.1.1 Access Password

The Access Password is a 32-bit value stored in Reserved Memory 20_h to $3F_h$ MSB first. The default value is all zeroes. Tags with a non-zero Access Password will require a reader to issue this password before transitioning to the secured state.

4.3.1.2 Kill Password

The Kill Password is a 32-bit value stored in Reserve Memory 00_h to $1F_h$, MSB first. The default value is all zeroes. A reader shall use a tag's kill password once to kill the tag and render it silent thereafter. A tag will not execute a kill operation if its Kill Password is all zeroes.

4.3.1.3 Memory Map Selection

Monza R6-P comes from the factory with space for a 128 bit EPC in the EPC bank and 32 bits of memory in the User bank. This memory corresponds to the memory map selection bit, M, being equal to one. The user may write this bit once. If the value is set to zero then the EPC bank will only support a 96 bit EPC, but the User bank will increase to 64 bits of memory. After a memory map is selected the memory map is locked and no further changes are permitted. In addition if any valid Lock command is issued to the tag the memory map will be locked.

4.3.1.4 Short Range

Monza R6-P comes with a short range capability to enhance consumer privacy. The short range bit in reserved memory may be written when the tag is in the secured state. When a reader writes the S bit to a one the tag will only respond when it is near the reader. Short range may be turned off by putting the tag into the secured state and writing the S bit to a zero.

4.3.1.5 AutoTune Disable and AutoTune Value

The AutoTune disable bit is in word 04_h, marked A in the memory map, and the AutoTune value, marked ATV[2:0] in word 14_h. The factory programmed value of the AutoTune disable bit is zero. The AutoTune value represents the tuning capacitance scale, from zero to four. A value of zero removes 80 fF of capacitance across the RF input of the tag and a value of four adds 100 fF across the RF input of the chip. See Table 4-13 for the mapping between AutoTune value and the change in input capacitance. A reader acquires the AutoTune value by issuing a single word *Read* command to word 14_h in the reserved memory bank. The AutoTune value is not writable.

To disable AutoTune a reader issues a Write command or a single word BlockWrite command to word 04_h. Only the bits for AutoTune disable, memory map selection and short range may change and the rest of bits in the payload will be ignored. If the tag's Reserved memory is locked then the AutoTune disable bit will also be locked.

When the AutoTune disable bit is zero AutoTune works as normal and when the bit is one AutoTune is overridden and the capacitance across the RF input is set to 0 fF. When AutoTune is disabled, the readout of AutoTune value does not represent the value of capacitance across the RF input to the tag.

Table 4-13 AutoTune Value

AUTOTUNE VALUE	CHANGE IN INPUT CAPACITANCE (FF)
0h	-80
1h	-40
2h	0
3h	+60
4h	+100

4.3.2 EPC Memory (EPC data, Protocol Control Bits, and CRC16)

As per the Gen 2 specification, EPC memory contains a 16-bit cyclic-redundancy check word (CRC16) at memory addresses 00_h to $0F_h$, the 16 protocol-control bits (PC) at memory addresses 10_h to $1F_h$, and an EPC value beginning at address 20_h.

The protocol control fields include a five-bit EPC length, a one-bit user-memory indicator (UMI), a one-bit extended protocol control indicator, and a nine-bit numbering system identifier (NSI). The UMI bit is set to a default value of
1 to indicate presence of user memory bank. The factory-programmed value is 3400_h.

The tag calculates the CRC16 upon power-up over the stored PC bits and the EPC specified by the EPC length field in the stored PC. For more details about the PC field or the CRC16, see the Gen 2 specification.

A reader accesses EPC memory by setting MemBank = 01_2 in the appropriate command, and providing a memory address using the extensible-bit-vector (EBV) format. The CRC-16, PC, and EPC are stored MSB first (i.e., the EPC's MSB is stored in location 20_h).

The EPC memory bank of Monza R6-P supports a maximum EPC size of 128 bits in the Default Memory Profile and a maximum EPC size of 96 bits in the Max User Memory Profile (see Table 2-1). The default configuration from the factory, however, is for a 96-bit EPC. It is possible to adjust the EPC size up or down from 96 bits, according to the parameters laid out in the Gen 2 standard. The EPC value written into the chip during factory

test is listed below in Table 4-14. The “X” nibbles in the pre-programmed EPC are pre-serialized values that follow the Impinj Monza Self-Serialization formula for Monza R6-P.

Table 4-14 EPC at Factory-Program

IMPINJ PART NUMBER	EPC VALUE PRE-PROGRAMMED AT THE FACTORY (HEX)
IPJ-W1710-K00	E280 1170 XXXX XXXX XXXX XXXX

4.3.3 Tag Identification (TID) Memory

The ROM-based Tag Identification memory contains Impinj-specific data. The Impinj MDID (Manufacturer Identifier) for Monza R6-P is 100000000001 (the location of the manufacturer ID is shown in the memory map tables in section 4.1, and the bit details are given in Table 4-5). Note that a logic 1 in the most significant bit of the manufacturer ID (as in the example bordered in solid black in the table) indicates the presence of an extended TID consisting of a 16-bit header and a 48-bit serialization. The 48-bit serialization has even parity as discussed in section 2.4.2. The Monza R6-P tag chip model number is located in the area bordered by the dashed line in TID memory row 10_h-$1F_h$ as shown in Table 4-15. The non-shaded bit locations in TID row 00_h-$0F_h$ store the EPCglobal™ Class ID (0xE2).

Table 4-15 TID Memory Details

MEMORY BANK DESCRIPTION	MEMORY BANK BIT ADDRESS	BIT NUMBER															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
10_2 TID (ROM)	50_h-$5F_h$	TID_SERIAL[15:0]															
	40_h-$4F_h$	TID_SERIAL[31:16]															
	30_h-$3F_h$	TID_SERIAL[47:32]															
	20_h-$2F_h$	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	10_h-$1F_h$	0	0	0	1	Monza R6-P Model Number											
						0	0	0	1	0	1	1	1	0	0	0	0
	00_h-$0F_h$	1	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0

4.3.4 User Memory

At the factory the User bank contains two 16-bit words at word address 0_h to 1_h. The User bank has individually controllable lock bits. When the memory map selection bit is set to zero the User bank is increased to four 16-bit words at word addresses 0_h to 3_h. When configured to this larger memory map the BlockPermalock command is accepted and there are two 32 bit blocks. Block zero is at word address 0_h to 1_h and block one is at word address 2_h to 3_h.

When the memory map is configured to Max User Memory Profile, the end user can use the combination of the BlockPermalock command and Lock command to create two blocks of memory, one of which is permanently locked and the other permanently unlocked. The BlockPermalock command must be issued first to lock one of the two blocks of user memory, then the Lock command must be issued to PermaUnlock the rest of the user memory. This is illustrated below for reference.

Table 4-16 User Memory Blocks

30_h-$3F_h$	Block 1	BlockPermalock on Block 1
20_h-$2F_h$		
10_h-$1F_h$	Block 0	PermaUnlock via Lock command on Block 0
00_h-$0F_h$		

5 ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed in this section may cause permanent damage to the tag. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this datasheet is not guaranteed or implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.1 Temperature

Several different temperature ranges will apply over unique operating and survival conditions. Table 5-17 lists the ranges that will be referred to in this specification. Tag functional and performance requirements are met over the operating range, unless otherwise specified.

Table 5-17 Temperature parameters

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	COMMENTS
Extended Operating Temperature	–40		+85	°C	Default range for all functional and performance requirements
Storage Temperature	–40		+85/125	°C	At 125C data retention is 1 year.
Assembly Survival Temperature			+150	°C	Applied for one minute
Temperature Rate of Change			4	°C / sec	During operation

5.2 Electrostatic Discharge (ESD) Tolerance

The tag is guaranteed to survive ESD as specified in Table 5-18.

Table 5-18 ESD Limits

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	COMMENTS
ESD			2,000	V	HBM (Human Body Model)

5.3 NVM Use Model

Tag memory is designed to endure 100,000 write cycles or retain data for 50 years.

6 ORDERING INFORMATION

Contact sales@impinj.com for ordering support.

PART NUMBER	FORM	PRODUCT	PROCESSING FLOW
IPJ-W1710-K00	Wafer	Monza R6-P tag chip	Padded, thinned (to ~109 µm), and diced

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